Experienced ASIC/FPGA Design and Verification Engineers

To join several ongoing projects in the SyoSil team, we are immediately looking for up to two engineers, preferably each with 3+ years of experience in ASIC/FPGA design and verification but recent graduates are also relevant.

You must have solid skills in RTL module design and verification, preferably using SystemVerilog and constrained random verification methodologies such as VMM or UVM. Additionally, you must be able to debug complex systems in a traditional FPGA/ASIC design simulation environment. The ability to understand complex test bench environments is a strong qualification.

You are preferably proficient with software development, using object oriented programming methods (C++, SystemVerilog or Python), and able to debug complex software systems in a traditional Linux based software environment using revision control systems (e.g. Git).

Your responsibilities will include a high degree of self-management of your own projects, and require you to interface directly with our customers, as well as internally in the SyoSil team.

We offer a competitive salary, and a flexible working environment meeting your personal work-life balance expectations. We invest significantly in the knowledge and expertise of the SyoSil team, making it possible for you to develop and maintain first class professional skills. This includes training and becoming proficient with ASIC tools from the top EDA vendors in the SyoSil partnership portfolio.

Candidates must have a relevant education as B.Sc. or M.Sc. in electrical engineering / computer science.

SyoSil is a leader in FPGA/ASIC design and verification solutions, including device firmware and tool development. We advice our clients on how to improve their design and verification methodologies, and deliver turn-key verification flows and Verification IP, based on industry standards such as SystemVerilog/UVM. Our clients include top European and U.S. semiconductor companies, all being respective leaders in their respective product segments (consumer, communication, automotive and surveillance).

We are a young and dynamic team of thirteen full time engineers working in an international environment, with very skilled and open-minded colleagues. Join our expanding team, soon to move to bigger facilities close to our existing address, located just 15 minutes by train from downtown Copenhagen.

For additional information, please contact: Jacob Sander Andersen (CTO), EMail: jacob <AT> syosil.com

Please send us your application including a detailed CV and university transcript no later than September 18th, 2016. The sooner the better!

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